REMARKS

The Reply is timely filed and responsive to the Office Action dated September 28, 2004.

In this Reply, claim 1 and 14 have been amended, and no claims have been cancelled. New claims 15 and 16 have been added. No new matter has been added.

In the Office Action, Claims 1-3 and 5-13 were rejected under 35 U.S.C. 102(b) as being anticipated by Kawai (US Patent 6,140,169), while claim 4 was rejected as being obvious over Kawai. Claims 1-13 were alternatively rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai et al. '169 as applied to the claims above, and further in view of Kolodzey et al. (US Patent 6,539,194) based on the assertion that it would have been "obvious to have oxidized the AlN gate insulator of Kawai for the purpose of enabling the resultant MOSFET to operate at significantly higher temperatures". Claim 14 was rejected under 3 U.S.C. 103(a) as being unpatentable over Kawai '169 as applied to the claims above, and further in view of Hong et al. (US Patent 6,469,357).

According to the Examiner in paragraph 2 of the Action Kawai discloses:

> various GaN-based enhancement-mode MOSFETS (i.e., MOSFETs that are in the off-state when the gate is not biased). See e.g. the third embodiment depicted in Figs. 9 and 10 which includes: a GaN comprising layer (GaInN electron transit layer 23(b)); a IIIGaN (electron supply) layer 23a that is less than 20 nm (e.g. 3 nm) thick (col. 89, lines 1-5); and an AlN gate insulating/dielectric film 4 that is preferably 1-10 nm thick (col. 12, lines 1-5, and may be 3 nm thick, e.g. col. 4, lines 34-36), and a gate electrode formed thereover.

Applicants first note that the characterization of the Kawai device does not includes the source and drain structure of the device, even though Applicants' claim 1 pending at the time of the Office Action recited "a source and a drain extending through said (Group III)$_x$Ga$_{1-x}$N layer into said GaN layer, said source and drain separated by a channel region". As will be clear after Applicants' description of Kawai, the device disclosed by Kawai is far from a typical MOS device, as it has no source and drain diffusion (only source and drain electrodes) and thus lacks

p-n junctions at the source to body and drain to body interfaces. Accordingly, Applicants respectfully note that the rejection of former claim 1 as stated above was improper.

Although not necessary to distinguish the claimed invention recited in original claim 1 from Kawai based on Kawai's lack of source and drain diffusions, Applicants have amended claim 1 to highlight other salient distinctions between the claimed invention and Kawai. Before reviewing the cited art, Applicants will first review the claimed invention as now recited in amended claim 1 (additions shown as underlined). Amended claim 1 recites a GaN based enhancement mode MOSFET, comprising a GaN comprising layer, and a (Group III)$_x$Ga$_{1-x}$N layer, where x is from 0 to 1, disposed on the GaN layer, a thickness of said (Group III)$_x$Ga$_{1-x}$N layer being less than 20 nm. A doped semiconductor source and a doped semiconductor drain extend through the (Group III)$_x$Ga$_{1-x}$N layer into the GaN layer. The source and drain are separated by a channel region comprising the (Group III)$_x$Ga$_{1-x}$N layer and the GaN layer, wherein a first p-n junction is formed where the source contacts the channel region and a second p-n junction is formed where drain contacts said channel region. A gate dielectric layer disposed over the channel region. A gate electrode overlapping the source and the drain is disposed on the gate dielectric, wherein the MOSFET is in an off-state when the gate is not biased.

As noted in paragraph 33 of Applicants' application regarding an n-channel enhancement mode MOSFET according to the invention, one important feature regarding Applicants' invention is the thin (Group III)$_x$Ga$_{1-x}$N layer ($0<x<1$) which permits formation of an enhancement mode device:

However, if a p-AlGaN layer 120 thicker than about 10 nm is used, the device performance will generally be degraded as compared to a thinner p-AlGaN layer 120 due to longer distance between the gate 110 and the inversion channel (not shown). If the p-AlGaN layer 120 comprises a thick undoped AlGaN layer, such as > 20 nm, an n-channel will generally be formed at the AlGaN/GaN interface due to the piezoelectric effect. This will result in the formation of a depletion mode n-channel MOSFET device.

Another significant feature in the invention is the use of a gate insulator which provides a close match in lattice constant with the underlying GaN comprising layer. A close match in lattice constant results in the underlying GaN comprising layer having a low density of low interface states, which allows an inversion channel to be formed (true enhancement mode operation). A poor lattice match results in a high density of interface states which leads to depletion mode operation. Preferred gate insulators of MgO and Sc_2O_3 have been found by the inventors to provide a good lattice match with GaN are now individually recited in new claims 15 and 16, respectively. As will be shown below, no cited reference discloses either of these gate dielectric layers.

Kawai is entitled "Method for manufacturing field effect transistor" and discloses a GaN-type field effect transistor exhibits a large input amplitude by using a gate insulating film. A channel layer and a gate insulating film are sequentially laminated on a substrate with a buffer layer therebetween. A gate electrode is formed on the gate insulating film. A *source electrode and a drain electrode* are disposed at the both sides of the gate electrode and are electrically connected to the channel layer via openings. The channel layer is formed from n-type GaN. The gate insulating film is made from AlN, which exhibits excellent insulation characteristics, thus increasing the Schottky barrier and achieving a large input amplitude. [italics for emphasis only].

Referring to any of the devices shown in figures provided by Kawai or disclosed in the Kawai application, such as Fig. 9 cited by the Examiner, Applicants note the source electrode 5 and drain electrode 6 are simply metal layers disposed on semiconducting electron supply layer 23(a) and contacting the same via opening 4b of the gate insulting film (col. 4; line 3-4). As noted in col. 4, lines 6-9 the source electrode 5 and drain electrode 6 as well as gate electrode 7

"are formed by sequentially laminating, for example, titanium (Ti), aluminum (Al), and gold (Au), from the upper surface of the substrate 1".

Moreover, as is clear from Fig. 9, the gate electrode 7 is "disposed on the gate insulating film 4 *between* the source electrode 5 and drain electrode 6" (col. 4; lines 4-6). Clearly, the gate electrode 7 does not overlap a source and drain diffusion as in a conventional MOS device, since Kawai discloses a metallic source electrode 5 and drain electrode 6, not a semiconducting source and drain diffusion.

Kawai asserts that they can adjust the n-type doping to get truly enhancement mode device. Even if true, in such a case, the device will not work well, because the gate can only modulate the semiconductor under it. The gate cannot modulate the semiconductor region between gate and source electrode 5 and gate and drain electrode 6. The parasitic resistance between gate and source electrode 5 and gate and drain electrode 6 will be very large, since the disclosed doping level is too low. The Kawai devices disclosed will also suffer another problem, namely punch through between source electrode 5 and drain electrode 6, since there is no pn junction blocking as compared to a conventional Si-based MOSFET or Applicants' claimed device.

In contrast to Kawai, the MOSFET recited in Applicants' amended claim 1 has a structure analogous to a conventional Si-based MOSFET (see Applicants' Fig. 1(a) or 1(b) which shows a gate electrode overlapping n+ source and n+ drain). Unlike Kawai's metallic source electrode and drain electrode, amended claim 1 recites a doped semiconductor source and a doped semiconductor drain extending through the (Group III)$_x$Ga$_{1-x}$N layer into the GaN layer (see N+ diffusions for source and drain in Applicants' Fig. 1(a) and (b)). Applicants' structure forms a first p-n junction is where the source contacts the channel region and a second p-n junction

where the drain contacts the channel region. Kawai does not form any p-n junctions, only Schottky contacts between the metal source and drain electrodes and the semiconductor. Applicants' claimed gate electrode is "overlapping said source and said drain" (again see overlap of gate electrode over source and drain diffusions in Applicants' Fig. 1(a) and (b)) in contrast to Kawai's gate electrode which is disposed between the source electrode 5 and drain electrode 6, but not overlapping source electrode 5 and drain electrode 6. Accordingly, Applicants submit that amended claim 1 clearly patentable over Kawai.

The other cited references do not make up for the deficiencies of Kawai noted above. Kolodzey discloses a method for making a metal-insulator-semiconductor field effect transistor (MISFET) having an oxidized aluminum nitride gate insulator formed on a silicon or gallium nitride substrate. The method of making the MISFET comprises the steps of depositing an aluminum nitride layer on the entire upper surface of the silicon or gallium nitride substrate. Subsequently, the aluminum nitride layer is oxidized to convert it into an oxidized aluminum nitride layer which acts as a gate insulator of the MISFET. Although devices disclosed by Kolodzey include GaN-based devices which appear to have a structure analogous to a conventional Si-based MOSFET, Kolodzey does not disclose or suggest an enhancement mode device, nor the layers recited by Applicants' in amended claim 1 to support such a device, such as Applicants' claimed "(Group III)$_x$Ga$_{1-x}$N layer, where x is from 0 to 1, disposed on said GaN layer, a thickness of said (Group III)$_x$Ga$_{1-x}$N layer being less than 20 nm". Moreover, Kolodzey is clearly not combinable with the unconventional FET disclosed by Kawai, except perhaps with respect to the gate insulator.

Hong discloses that a single crystal, single domain oxide layer of thickness less than 5 nm can be grown on a (100) oriented GaAs-based semiconductor substrates and merely speculates

that similar epitaxial oxide can be grown on GaN and GaN-based semiconductors. The oxide typically is a rare earth oxide of the Mn_2O_3 structure (e.g., Gd_2O_3). The oxide/semiconductor interface can be of high quality, with low interface state density, and the oxide layer can have low leakage current and high breakdown voltage. The low thickness and high dielectric constant of the oxide layer result in a MOS structure of high capacitance per unit area. Such a structure advantageously forms a GaAs-based MOS-FET.

Although the Examiner asserts that Hong discloses Sc_2O_3, in col. 6, lines 31 , 54 and 60, Applicants respectfully point out that this is not the case. Although Sc is disclosed, Sc is disclosed as a rare earth (RE) for use in a mixed oxide film having the formula $Ga_xA_yO_z$, where Sc can be A (see lines 19-24). Thus, the dielectric Sc_2O_3 is not disclosed or suggested by Hong.

Although Hong briefly mentions GaN-based devices, he only teaches GaAs-based devices. Even assuming *arguendo* that devices disclosed by Hong include GaN-based devices, such GaN-based devices would appear to have a structure analogous to a conventional Si-based MOSFET. Again assuming *arguendo* that devices disclosed by Hong include GaN-based devices, like Kolodzey, Hong does not does not disclose or suggest an enhancement mode device, nor the layers recited by Applicants' in amended claim 1 to support such a device, such as Applicants' claimed "(Group III)$_x$Ga$_{1-x}$N layer, where x is from 0 to 1, disposed on said GaN layer, a thickness of said (Group III)$_x$Ga$_{1-x}$N layer being less than 20 nm". Moreover, Hong is clearly not combinable with the unconventional FET disclosed by Kawai, except perhaps with respect to the gate insulator. Accordingly, amended claim 1 and all claims dependent thereon are patentable claims.

Several claims include independently patentable limitations. Claim 15 recites the gate dielectric layer comprises MgO, while claim 16 recites the gate dielectric layer comprises Sc_2O_3. Neither of these gate insulators are disclosed or suggested in the references cited.

Applicants have made every effort to present claims which distinguish over the cited art, and it is believed that all claims are now in condition for allowance. However, Applicants request that the Examiner call the undersigned (direct line 561-671-3662) if anything further is required by the Examiner prior to issuance of a Notice of Allowance for all claims.

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Respectfully submitted,

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